(Effective from the academic session 2020-21)

GURUKULA KANGRI VISHWAVIDYALAYA, HARIDWAR

Faculty of Engineering & Technology

Electronics & Communication Engineering

B. Tech. Second Year

Syllabus in accordance with AICTE Model Curriculum

SEMESTER-III

DSC/SEC/ DSE/AEC	SUBJECT	PERIODS			EVALUATION SCHEME				Subject Total	Credits
					SESSIONAL EVALUATION			EXAM ESE		
		L	T	P	CT	TA	Total			
THEORY										
BEM-C302	Engineering Mathematics- III	3	1	0	20	10	30	70	100	4
BET-C305	Analog Communication	3	0	0	20	10	30	70	100	3
BCE-C305	Data Structure-I	3	0	0	20	10	30	70	100	3
BCE-C306 CSE/EC	Computer Architecture and Organization	3	0	0	20	10	30	70	100	3
BET-C306	Digital System Design	3	0	0	20	10	30	70	100	3
		TOTAL CREDITS								16
PRACTICAL										
BET-C354	Analog Communication Lab	0	0	2	10	5	15	35	50	1
BCE-C355	Data Structure-I Lab	0	0	2	10	5	15	35	50	1
BET-C355	Digital System Design Lab	0	0	2	10	5	15	35	50	1
BET-S359	Summer Training and Internship Program-I/mini project (3-4 weeks)	To be pursued during summer vacation, submit a certificate of completion in the department (in summer break after II semester exam and will be assessed during III semester)							50	1
		TOTAL CREDITS								4
TOTAL		15	1	6	130	65	195	455	700	20

Effective from the session 2020-21
BEM-C302
ENGINEERING MATHEMATICS- III

MM : 100 **Sessional : 30**
Time : 3 Hr **ESE : 70**
L T P **Credit :4**
3 1 0

NOTE: The question paper shall consist of two sections (Sec.-A and Sec.-B). Sec.-A shall contain ten questions of six marks each and student shall be required to attempt five questions Sec.-B shall contain eight descriptive type questions of ten marks each and students shall be required to attempt any four questions. Question shall be uniformly distributed from the entire syllabus. The previous year paper /model paper can be used as a guideline and the following syllabus should be strictly followed while setting the question paper.

UNIT I

Laplace Transform: Laplace transform of elementary functions. Shifting theorems. Transform of derivatives. Differentiation and Integration of transforms. Heaviside unit step and Dirac Delta functions. Convolution theorem. Solution of ordinary linear differential equations used in Mechanics, Electric circuits and Bending of beams.

UNIT II

Fourier Transforms : Definition of Fourier transform, Fourier sine and cosine transforms. Fourier integral formula. Applications to solutions of boundry value problems.

UNIT III

Z - transform : Definition, Linearity property, Z - transform of elementary functions, Shifting theorems, Initial and final value theorem, Convolution theorem, Inversion of Z - transforms, Solution of difference equations by Z - transforms.

UNIT IV

Functions of a Complex Variable - I : Analytic functions, C-R equations and harmonic functions, Line integral in the complex plane, Cauchy's integral theorem, Cauchy's integral formula for derivatives of analytic functions, Liouville's theorem.

UNIT V

Functions of a Complex Variable - II : Representation of a function by power series, Taylor's and Laurent's series, Singularities, zeroes and poles, Residue theorem, evaluation of real integrals of type $\int_{o}^{2\pi} f(\cos\theta, \sin\theta)d\theta$ and $\int_{-\infty}^{\infty} f(x)/F(x)dx$, Conformal mapping and bilinear transformations.

References

1. Prasad C., Advanced mathematics for Engineers, Prasad Mudranalaya
2. Schaum outline Series, Integral Transform,TMH
3. Grewal B.S., Higher Engineering Mathematics, Khanna, New Delhi, 2000
4. Brancewel, Fourier Transforms and their applications, McGraw
5. Kreyszig E., Advanced Engineering Mathematics, John Wiley, New York, 1999

Course Outcomes

The objective of this course is to familiarize the prospective engineers with techniques in Laplace transform, Fourier transform, Z- transform and complex variables. It aims to equip the students to deal with advanced level of mathematics and applications that would be essential for their disciplines.

The students will learn:

- The mathematical tools needed in evaluating multiple integrals and their usage.
- The effective mathematical tools for the solutions of different transform that model physical processes.
- The tools of differentiation and integration of functions of a complex variable that are used in various techniques dealing engineering problems.

Effective from the session 2020-21
BCE-C305
DATA STRUCTURE – I

MM : 100 **Sessional : 30**
Time : 3 Hr **ESE : 70**
L T P **Credit :3**
3 0 0

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UNIT I

Structures: Structures definition, giving value to members, structure initialization, array of structures, array within structures, structures within structures, structures and functions,StructurePointrers.
File Handling: Creating and Deleting a File, Updating File, Copying File, Searching & Sorting in a File.
Complexity: Algorithm Complexity and Time-Space trade-off.

UNIT II

Stack: Array representation and Implementation of stack, Operations on stack: Push & Pop, Array representation of Stack, Linked representation of Stack, Operation associated with stacks, Application on stack: Conversion of Infix to Prefix and Postfix Expressions, Evaluation of Postfix expression using stack.
Queues: Array and linked representation and implementation of queues, Operations on Queue: Create, Add, Delete, Full and Empty. Circular queue, Deque and Priority Queue.

UNIT III

Linked List: Representation and Implementation of Singly Linked List, Two-way Header List, Traversing and Searching of Linked List, Overflow and Underflow, Insertion and Deletion to/from Linked List, Insertion and Deletion Algorithms, Doubly linked List, Linked List in Array, Polynomial representation and addition, Generalized linked list, Garbage Collection and Compaction.

UNIT IV

Trees: Basic terminology, Binary Trees, Binary Tree Representation, Algebraic Expressions, Complete Binary Tree. Extended Binary Trees, Array and Linked representation of Binary trees, Traversing Binary trees.
Binary Search Tree: Binary Search Tree (BST), Insertion and Deletion in BST, Complexity of search algorithm, Path Length, AVL Tree, B-trees.

UNIT V

Searching and Hashing: Sequential Search, Comparison and Analysis, Hash table, Hash Functions, Collision Resolution Strategies, Hash Table Implementation.
Sorting: Insertion Sort, Bubble Sorting, Quick Sort, Two way Merge Sort, Heap Sort, Sorting on Different Keys, Practical consideration for Internal Sorting.
File Structures: Physical Storage Media File Organization, Organization of records into Blocks, Sequential Files, Indexing and Hashing, Primary indices, Secondary indices, B+ Tree index Files, B Tree index Files, Indexing and Hashing Comparisons.

References

1. Horowitz and Sahani, Fundamentals of Data Structure, Galgotia.
2. R.Kruseetal, Data Structures and Program Design in C, Pearson Education.
3. A M Tenenbaumetal, Data Structure using C & C++, PHI.
4. Lipschutz, Data Structure, TMH.
5. K. Loudon, Mastering Algorithms with C, Sheoff Publisher & Distributors.
6. Bruno R Preiss, Data Structures and Algorithms with Object Oriented Design Pattern in C++, John Wiley & Sons, Inc.
7. YashwantKanetkar, Pointers in C, BPB

Course outcomes

1. For a given algorithm student will able to analyze the algorithms to determine the time and computation complexity and justify the correctness.
2. For a given Search problem (Linear Search and Binary Search) student will able to implement it.
3. For a given problem of Stacks, Queues and linked list student will able to implement it and analyze the same to determine the time and computation complexity.
4. Student will able to write an algorithm Selection Sort, Bubble Sort, Insertion Sort, Quick Sort, Merge Sort, Heap Sort and compare their performance in term of Space and Time complexity.
5. Student will able to implement Graph search and traversal algorithms and determine the time and computation complexity.

Effective from the session 2020-21
BCE-C306
COMPUTER ARCHITECHURE AND ORGANIZATION

MM : 100 **Sessional : 30**
Time : 3 Hr **ESE : 70**
L T P **Credit :3**
3 0 0

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UNIT I

Register Transfer Language, Bus and Memory Transfers, Bus Architecture, Bus Arbitration, Arithmetic Logic, Shift Micro-operation, Arithmetic Logic Shift Unit, Arithmetic Algorithms (addition, subtraction, Booth's Multiplication), IEEE standard for Floating point numbers.

UNIT II

Control Design: Hardwired & Micro Programmed Control Unit, Fundamental Concepts (Register Transfers, Performing of arithmetic or logical operations, Fetching a word from memory, storing a word in memory), Execution of a complete instruction, Multiple-Bus organization, Microinstruction, Microprogram sequencing, Wide-Branch addressing, Microinstruction with Next-address field, Prefetching Microinstruction.

UNIT III

Processor Design: Processor Organization: General register organization, Stack organization, Addressing mode, Instruction format, Data transfer & manipulations, Program Control, Reduced Instruction Set Computer (RISC), Complex Instruction Set Computer (CISC).

UNIT IV

Input-Output Organization: I/O Interface, Modes of transfer, Interrupts & Interrupt handling, Direct Memory access, Input-Output processor, Serial Communication.

UNIT V

Memory Organization: Memory Hierarchy, Main Memory (RAM and ROM Chips), organization of 2D, Auxiliary memory, Cache memory, Virtual Memory, Memory management hardware.

References

1. M. Mano, Computer System Architecture, PHI
2. Vravice, Zaky&Hamacher, Computer Organization, TMH Publication
3. Tannenbaum, Structured Computer Organization, PHI
4. Stallings, Computer Organization, PHI
5. John P.Hayes, Computer Organization, McGraw Hill

Course outcomes

1. Draw the functional block diagram of a single bus **architectureofacomputeranddescribethefunctionofthe** instruction execution cycle, RTL interpretation of instructions, addressing modes, instruction set.
2. **Write** assembly language program for specified microprocessor for computing 16 bit multiplication, division and I/O device interface (ADC, Control circuit, serial port communication).
3. Write a flowchart for Concurrent access to memory and cache coherency in **ParallelProcessors** and describe the process.
4. Given a CPU organization and instruction, design a memory module and analyze its operation by interfacing with the CPU.
5. Given a CPU organization, assess its performance, and apply design techniques to enhance performance using pipelining, parallelism and RISC methodology

Effective from the session 2020-21
BET-C305
ANALOG COMMUNICATION

MM : 100 **Sessional : 30**
Time : 3 Hr **ESE : 70**
L T P **Credit :3**
3 0 0

NOTE: The question paper shall consist of two sections (Sec.-A and Sec.-B). Sec.-A shall contain ten questions of six marks each and student shall be required to attempt five questions Sec.-B shall contain eight descriptive type questions of ten marks each and students shall be required to attempt any four questions. Question shall be uniformly distributed from the entire syllabus. The previous year paper /model paper can be used as a guideline and the following syllabus should be strictly followed while setting the question paper.

UNIT I

Signals and its Representation: Review of Fourier transform, Signal transmission through linear system, Signal distortion in transmission, Time domain versus Frequency Domain, Application of Delta function in Fourier Transform calculations Fourier transform of periodic signals.

UNIT II

Linear Modulation, Amplitude modulation, generation and demodulation of AM, Wave, suppressed carrier modulation, DSB-SC modulation, and its generation and demodulation, SSB-SC modulation, Exponential modulation, modulation F.M. waves, generation of F.M. waves, De-emphasis and Pre-emphasis filtering.

UNITIII

A.M. and F.M. transmitters, SSB transmission, F.M. transmitter, IC AM and FM standard transmitter.

UNIT IV

A.M. and F.M. Receivers, Superhetrodyne receivers, the complete A.M. receiver system, SSB receiver, F.M. receiver, Introduction To Television, Different Modulations Used In Television Transmission.

UNITV

Pulse Analog Modulation, Practical Sampling, Analog pulse modulation, Time Division multiplexing (TDM) Synchronization in pulse modulated system, Noise in Continuous-wave modulation, baseband system, noise calculation in communication system noise in A.M and angle modulated system.

References

1. Chakrabarti------ Analog and digital Communication-Dhanpatrai& Com.
2. Wayne Tomasi---Electronic Communications Systems-Pearson Education Asia Publisher.
3. Taub, H., Shillmg D.L. ---Principles of Communication Systems-Tata-McGraw Hill, N.D.
4. B.P. Lathi,"Modern Digital & Analog Communication Systems", Oxford University Press.
5. SimonHaykin / "Communication Systems" / John Wiley / 4th Ed.

Course Outcomes:

1. Analyze and compare different analog modulation schemes for their efficiency and bandwidth
2. Analyze the behavior of a communication system in presence of noise

Effective from the session 2020-21
BET-C306
DIGITAL SYSTEM DESIGN

MM : 100 **Sessional : 30**
Time : 3 Hr **ESE : 70**
L T P **Credit :3**
3 0 0

NOTE: The question paper shall consist of two sections (Sec.-A and Sec.-B). Sec.-A shall contain ten questions of six marks each and student shall be required to attempt five questions Sec.-B shall contain eight descriptive type questions of ten marks each and students shall be required to attempt any four questions. Question shall be uniformly distributed from the entire syllabus. The previous year paper /model paper can be used as a guideline and the following syllabus should be strictly followed while setting the question paper.

UNIT I

Number System: Representation of negative numbers, 9's and 1's complement, 10's and 2's complement, arithmetic using 2's complement. BCD Code, Gray Code, Excess-3 Code, Introduction to Boolean algebra, Truth table verification of various gates, Realization of Switching functions with gates.
K- Map: Representation up to 4 variables, simplification and realization of various functions using gates, Tabular Method, Combinational logic and design procedure.

UNIT II

Combinational logic Circuits: Arithmetic circuits, Half and Full adder, Subtractors, BCD adders, Code Conversion, 4 bit Magnitude Comparator (IC -7485), Cascading of IC 7485, Decoder, Multiplexer, Demultiplexers, Encoders. Parallel Binary adder, IC 7483, 4-bit Binary parallel adder/subtractor,

UNIT III

Sequential Logic Circuits: Flip Flops, S-R latch, gated latches, Edge triggered Flip Flops, Master-slave Flip Flops, Conversion of flip flops, Analysis of clocked sequential circuits, Design of synchronous circuits, State transition diagram, state reduction and assignment.

UNIT IV

Counters: Design of Asynchronous and Synchronous Counters, Two bits & four bits up & down counters and their design, Shift registers, Serial & Parallel data transfer, Shift left/Right register, Shift Register applications.

UNIT V

Logic Families: Diode switching, Transistors as a switching element, MOS as a digital circuit element, concept of transfer characteristics, input characteristics and output characteristics of logic gates, fan in, fan out, noise margin, Logic families: TTL, IIL, ECL, NMOS, & CMOS, Open collector outputs.

Reference

1. M.Morris Mano, Digital Design, PHI
2. R.P.Jain, Modern Digital electronics, TMH
3. A.Anand Kumar, Fundamentals of Digital Circuits, PHI
4. Lee S.C, Modern Switching Theory and Digital design, PHI
5. Greenfield J.D., Practical Digital design using ICs, John Wiley.

Course outcomes:

At the end of this course students will demonstrate the ability to

1. Design and analyze combinational logic circuits
2. Design & analyze modular combinational circuits with MUX/DEMUX, Decoder, Encoder
3. Design & analyze synchronous sequential logic circuits

Effective from the session 2020-21
BET-C354
ANALOG COMMUNICATION LAB

MM : 50 **Sessional : 15**
Time : 2Hr **ESE : 35**
L T P **Credit : 1**
0 0 2

LIST OF EXPERIMENT:

1. To study Amplitude modulation using a transistor and determine depth of modulation.
2. To study envelope detector for demodulation of AM signal and observe diagonal peak clipping effect.
3. To study frequency modulation using reactance modulator.
4. Study of frequency modulation using varactor modulator.
5. Narrow band FM generator using Armstrong method.
6. Study of Foster- Seely discriminator.
7. Generation of DSB-SC signal using balanced modulator.
8. Generation of single side band signal.
9. Study of phase lock loop and detection of FM signal using PLL.
10. Measurement of noise figure using a noise generator.
11. Study of super heterodyne AM receiver and measurement of sensitivity, selectivity & fidelity.
12. Study and demonstration of active filter (low pass, high pass, and band pass type).

NOTE

1. In practical examination the student shall be required to perform one experiment.
2. A teacher shall be assigned 20 students for daily practical work in laboratory.
3. No batch for practical class shall consist of more than 20 students.
4. The number of students in a batch allotted to an examiner for practical examination shall not exceed 20 students.
5. Addition/deletion in above list may be made in accordance with the facilities available with the approval of H.O.D./Dean.

Effective from the session 2020-21
BCE-C355
DATA STRUCTURE – I LAB

MM : 50 **Sessional : 15**
Time : 2Hr **ESE : 35**
L T P **Credit : 1**
0 0 2

Write Program in C

1. Array implementation of Stack.
2. Array implementation of Queue.
3. Array implementation of Circular Queue.
4. Implementation of Linked List.
5. Implementation of Circular Linked List
6. Implementation of Doubly Linked List
7. Implementation of Stack using list.
8. Implementation of Queue using list.
9. Implementation of Binary Search Tree, Tree Traversal.
10. Insertion and Deletion in BST.
11. Implementation of Searching and Sorting Algorithms.
12. Sort a double linked list.

NOTE

1. In practical examination the student shall be required to perform one experiment.
2. A teacher shall be assigned 20 students for daily practical work in laboratory.
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4. The number of students in a batch allotted to an examiner for practical examination shall not exceed 20 students.
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Effective from the session 2020-21
BET-C355
DIGITAL SYSTEM DESIGN LAB

MM : 50 **Sessional : 15**
Time : 2Hr **ESE : 35**
L T P **Credit : 1**
0 0 2

LIST OF EXPERIMENTS :

1. To verify the truth tables of various types of gates using IC 7400.
2. To verify the truth tables of Multiplexer & also implement a function using Multiplexer.
3. To design & verify the truth table of half & full adder.
4. To design & verify the truth table SR flip-flop using NOR/NAND gates.
5. To design & verify the truth table JK flip-flop using NOR/NAND gates.
6. To design & study Counters.
7. To design & study Shift registers.
8. To verify the truth tables of de Multiplexer.

NOTE

1. In practical examination the student shall be required to perform one experiment.
2. A teacher shall be assigned 20 students for daily practical work in laboratory.
3. No batch for practical class shall consist of more than 20 students.
4. The number of students in a batch allotted to an examiner for practical examination shall not exceed 20 students.
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Effective from the session 2020-21
BET-S359
Summer Training and Internship Program-I/mini project
(3-4 weeks)

MM : 50 **Sessional : 50**
Time :0 Hr **ESE : 0**
L T P **Credit : 1**
0 0 0

Guidelines:

1. The internship certificate will have to be submitted in the departmentafter summer vacation for evaluation.
2. Students can choose to do internship or mini project or industrial training.
3. The mini-project is a team activity having 2-3 students in a team. This is electronic productdesign work with a focus on electronic circuit design.
4. The mini project may be a complete hardware or a combination of hardware and software.The software part in mini project should be less than 50% of the total work.
5. Mini Project should cater to a small system required in laboratory or real life.
6. It should encompass components, devices, analog or digital ICs, micro controller with whichfunctional familiarity is introduced.
7. After interactions with course coordinator and based on comprehensive literature survey/need analysis, the student shall identify the title and define the aim and objectives of mini-project.
8. Student is expected to detail out specifications, methodology, resources required, criticalissues involved in design and implementation and submit the proposal within first week ofthe semester.
9. The student is expected to exert on design, development and testing of the proposed work as per the schedule.
10. Art work and Layout should be made using CAD based PCB simulation software. Dueconsiderations should be given for power requirement of the system, mechanical aspects forenclosure and control panel design.
11. Completed mini project and documentation in the form of mini project report is to be submitted at the end of semester.
12. The tutorial sessions should be used for discussion on standard practices used for electronic circuits/product design, converting the circuit design into a complete electronic product, PCB design using suitable simulation software, estimation of power budget analysis of the product, front panel design and mechanical aspects of the product, and guidelines for documentation/report writing.

Course Outcomes:

At the end of the course, students will demonstrate the ability to:

1. Conceive a problem statement either from rigorous literature survey or from the requirements raised from need analysis.
2. Design, implement and test the prototype/algorithm in order to solve the conceived problem.
3. Write comprehensive report on mini project work.